We Claim:

1. A semiconductor interconnect comprising:

a substrate having a first side and an opposing second side;

a first contact on the first side of the substrate, the first contact comprising a recess at least partially covered by a conductive layer and configured to retain and electrically engage a second contact on a semiconductor component; and

a conductive member comprising a laser machined opening in the substrate extending from the conductive layer to a second side of the substrate, the opening at least partially filled with a conductive material in contact with the conductive layer.

2. The interconnect of claim 1 wherein the conductive material comprises a metal or a conductive polymer.

3. The interconnect of claim 1 wherein a center line of the conductive member is conincident to a center line of the first contact.

4. The interconnect of claim 1 wherein a center line of the conductive member is offset from a center line of the first contact.

5. The interconnect of claim 1 wherein the conductive member includes a pad on the second side of the substrate.

6. The interconnect of claim 1 wherein the conductive member includes a contact ball on the second side of the substrate.

7. A semiconductor interconnect comprising:

a substrate having a first side and an opposing second side;

a first contact on the first side of the substrate, the first contact comprising a penetrating member covered by a conductive layer, the penetrating member configured to penetrate and electrically engage a second contact on a semiconductor component; and

a conductive member comprising a laser machined opening in the substrate with an insulating layer thereon, the opening extending from the conductive layer to a second side of the substrate, the opening at least partially filled with a conductive material.

8. The interconnect of claim 7 wherein the first contact comprises a recess at least partially covered by the conductive layer and configured to retain the second contact.

9. The interconnect of claim 7 wherein the first contact comprises a projection at least partially covered by the conductive layer and configured to electrically engage the second contact while maintaining separation of the component and interconnect.

10. The interconnect of claim 7 wherein the conductive member includes a pad and a contact ball on the second side of the substrate.

11. A semiconductor interconnect comprising:

a substrate having a first side and an opposing second side;

a contact on the first side of the substrate, the contact comprising a recess covered by a conductive layer,

the recess configured to retain and electrically engage a bumped contact on a semiconductor component;

a laser machined opening located within the recess and extending through the substrate to the second side;

an insulating layer formed on an inside surface of the opening; and

a conductive material deposited on the inside surface of the opening in contact with the conductive layer.

12. The interconnect of claim 11 wherein the conductive material comprises a metal filling the opening.

13. The interconnect of claim 11 wherein the conductive material comprises a metal layer on the inside surface configured for electrical engagement by an electrical connector on a test apparatus.

14. The interconnect of claim 11 wherein the conductive material comprises a conductive polymer filling the opening.

15. The interconnect of claim 11 wherein the conductive material includes a pad and a contact ball located proximate to the second surface.

16. The interconnect of claim 11 wherein the recess comprises a stepped surface configured to electrically engage first or second bumped contacts having a different diameter.

17. A semiconductor interconnect comprising:

a substrate having a first side and an opposing second side;

a first contact on the first side of the substrate, the contact comprising a projection covered by a conductive layer, the projection configured to electrically engage a

second contact on a semiconductor component while maintaining separation of the component and substrate;

a laser machined opening proximate to the first contact and extending through the substrate to the second side;

an insulating layer formed on an inside surface of the opening; and

a conductive material deposited on the inside surface of the opening in contact with the conductive layer.

18. The interconnect of claim 17 further comprising a penetrating member on the projection configured to penetrate the second contact to a limited penetration depth.

19. The interconnect of claim 17 further comprising a contact ball on the conductive material proximate to the second surface.

20. The interconnect of claim 17 further comprising a pad on the conductive material proximate to the second surface.

21. The interconnect of claim 17 wherein the conductive material comprises a material selected from the group consisting of metal and conductive polymers.

22. A method for fabricating a semiconductor interconnect comprising:

providing a substrate having a first side and an opposing second side;

forming a recess in the first side, the recess sized to retain a bumped contact on a semiconductor component;

depositing a conductive layer within the recess configured to electrically engage the bumped contact;

forming an opening within the recess, the opening extending through the substrate to the second side; and

depositing a conductive material on an inside surface of the opening in contact with the conductive layer.

23. The method of claim 22 wherein forming the opening comprises laser machining.

24. The method of claim 22 further comprising forming a penetrating member in the recess at least partially covered by the conductive layer and configured to penetrate the contact.

25. The method of claim 22 further comprising forming a pad on the second surface in electrical contact with the conductive material.

26. The method of claim 22 further comprising forming a pad on the second surface in electrical contact with the conductive material and offset from a centerline of the recess.

27. The method of claim 22 further comprising forming a contact ball on the second surface in electrical contact with conductive material.

28. The method of claim 22 further comprising forming a contact ball on the second surface in electrical contact with the conductive material and offset from a centerline of the recess.

29. A method for fabricating a semiconductor interconnect comprising:

providing a substrate having a first side and an opposing second side;

forming a first contact on the first side, the first contact comprising a projection at least partially covered with a conductive layer configured to electrically engage a second contact on a semiconductor component;

forming an opening through the substrate extending from the conductive layer to the second side of the substrate; and

depositing a conductive material on an inside surface of the opening in contact with the conductive layer.

30. The method of claim 29 wherein forming the opening comprises laser machining.

31. The method of claim 29 further comprising forming a penetrating member on the projection at least partially covered by the conductive layer and configured to penetrate the second contact.

32. The method of claim 29 further comprising forming a pad on the conductive material proximate to the second surface.

33. The method of claim 29 further comprising forming a pad on the conductive material proximate to the second surface and offset from a center line of the projection.

34. The method of claim 29 further comprising forming a contact ball on the conductive material proximate to the second surface.

35. The method of claim 29 further comprising forming a contact ball on the conductive material proximate to the

second surface and offset from a center line of the projection.

36. A method for fabricating a semiconductor interconnect comprising:

providing a substrate having a first side and an opposing second side;

forming a first contact on the first side, the first contact comprising a conductive layer configured to electrically engage a second contact on a semiconductor component;

laser machining an opening through the substrate to the second side;

forming an insulating layer on an inside surface of the opening; and

depositing a conductive material on the insulating layer in contact with the conductive layer.

37. The method of claim 36 further comprising forming a penetrating member on the first contact the penetrating member at least partially covered by the conductive layer and configured to penetrate the second contact.

38. The method of claim 36 wherein the second contact comprises a bump and the first contact comprises a recess having the opening located therein.

39. The method of claim 36 wherein the second contact comprises a planar pad and the first contact comprises a projection configured to maintain separation of the component and substrate.

40. The method of claim 36 wherein the second contact comprises a bump first contact comprises a stepped recess

configured to retain the second contact or a third bumped contact.

41. A method for fabricating a semiconductor interconnect comprising:

providing a substrate having a first side and an opposing second side;

forming a recess in the first side, the recess sized to retain a bumped contact on a semiconductor component;

forming a penetrating member in the recess configured to penetrate the bumped contact;

depositing a conductive layer within the recess and on the penetrating member, the conductive layer configured to electrically engage the bumped contact;

laser machining an opening through the recess and the substrate to the second side; and

depositing a conductive material on an inside surface of the opening in contact with the conductive layer.

42. The method of claim 41 further comprising following laser machining forming an electrically insulating layer on the inside surface of the opening and depositing the conductive material on the inside surface.

43. The method of claim 41 wherein depositing the conductive material comprises chemically vapor depositing a metal into the opening.

44. The method of claim 41 wherein depositing the conductive material comprises stenciling a conductive polymer into the opening.

45. The method of claim 41 further comprising forming a pad on the second side in electrical contact with the conductive material.

46. The method of claim 41 further comprising forming a contact ball on the second side in electrical contact with the conductive material.

47. The method of claim 41 further comprising attaching the interconnect to a semiconductor die to form a chip scale package.

48. The method of claim 41 further comprising mounting the interconnect to a test carrier configured to house the component for testing.

49. The method of claim 41 wherein the component comprises a wafer and further comprising mounting the interconnect to a wafer handler configured to test the wafer.

50. A test carrier for a semiconductor component comprising:

a base comprising a terminal contact;

an interconnect mounted to the base having a first side and an opposing second side;

a first contact on the first side of the interconnect, the first contact comprising a conductive layer configured to electrically engage a second contact on the semiconductor component;

a conductive member comprising a laser machined opening in the interconnect extending from the conductive layer to the second side, the opening at least partially filled with a conductive material in contact with the conductive layer; and

an electrical connector on the base in electrical communication with the terminal contact and the conductive member.

51. The test carrier of claim 50 wherein the conductive member includes a first pad and the electrical connector comprises a second pad in electrical contact with the first pad.

52. The test carrier of claim 50 wherein the conductive member includes a first pad and the electrical connector comprises a second pad bonded to the first pad.

53. The test carrier of claim 50 wherein the conductive member includes a contact ball and the electrical connector comprises a second recess in electrical contact with the first pad.

54. The test carrier of claim 50 wherein the conductive member comprises a metal layer on an inside surface of the opening and the electrical connector comprises a bump having a portion in electrical contact with the metal layer.

55. The test carrier of claim 50 wherein the electrical connector comprises a conductive polymer on the substrate bonded to the conductive member.

56. The test carrier of claim 50 wherein the first contact comprises a recess and the opening extends through the recess.

57. The test carrier of claim 50 wherein the first contact comprises a projection having a penetrating member for penetrating the second contact.

58. A semiconductor probe card comprising:

a probe card substrate;

an interconnect mounted to the probe card substrate having a first side and an opposing second side;

a first contact on the first side of the interconnect, the first contact comprising a conductive layer configured to electrically engage a second contact on a semiconductor wafer;

a conductive member comprising a laser machined opening in the interconnect extending from the conductive layer to the second side, the opening at least partially filled with a conductive material in contact with the conductive layer; and

a pad on the second side in electrical contact with the conductive member, the pad configured for electrical engagement with an electrical connector.

59. The probe card of claim 58 wherein the first contact comprises a recess and the opening extends through the recess.

60. The probe card of claim 58 wherein the first contact comprises a projection having a penetrating member for penetrating the second contact.

61. The probe card of claim 58 wherein the first contact comprises a recess having a penetrating member form penetrating the second contact.

62. The probe card of claim 58 wherein the opening includes a longitudinal axis and the pad has a centerline offset the axis.

63. A semiconductor package comprising:

a semiconductor die having a face with a bumped contact thereon;

an interconnect placed on the face and having a first side and an opposing second side;

a contact on the first side, the contact comprising a recess covered by a conductive layer bonded to the bumped contact;

a laser machined opening through the interconnect to the second side;

a conductive member formed in the opening in contact with the conductive layer; and

a pad formed on the second side in contact with the conductive member.

64. The package of claim 63 further comprising an underfill layer formed between the interconnect and the die.

65. The package of claim 63 wherein the conductive member comprises a conductive polymer deposited in the opening.

66. The package of claim 63 further comprising a contact ball on the pad.

67. A semiconductor package comprising:

an interconnect having a first side and an opposing second side, the interconnect including a first opening extending from the first side to the second side, and a conductor on the second side;

a semiconductor die having a face with a bumped contact thereon, the die placed on the first side with the bumped contact bonded through the first opening to the conductor;

a laser machined opening extending from the first side to the second side;

a conductive member formed in the opening in contact with the conductor; and

a pad on the second side in electrical communication with the conductive member and configured for electrical contact with a second semiconductor package.

68. The package of claim 67 further comprising a bump on the conductor configured for electrical contact with a second pad on the second semiconductor package.

69. The package of claim 67 and further comprising the second package stacked on the first package to form a multi chip module.

70. A multi chip module comprising:

a first semiconductor package and a second semiconductor package;

each semiconductor package comprising a semiconductor die and an interconnect attached to the die, the interconnect comprising a laser machined opening and a conductive member formed in the opening;

the first package stacked on the second package with a first conductive member on the first package in electrical communication with a second conductive member on the second package.

71. The module of claim 70 wherein the first conductive member includes a contact ball bonded to the second conductive member.

72. The module of claim 70 wherein each semiconductor package is mounted to the interconnect in a chip on board configuration.

73. The module of claim 70 wherein each semiconductor package is mounted to the interconnect in a flip chip configuration.

74. The module of claim 70 wherein the interconnect includes raised contact members configured to electrically engage bond pads on the die.

75. A multi chip module comprising:

an interconnect having a first side and an opposing second side;

a plurality of first contacts on the first side of the interconnect, the plurality of first contacts comprising conductive layers;

a plurality of conductive members comprising laser machined openings in the interconnect extending from the conductive layers to the second side, the openings at least partially filled with a conductive material in contact with the conductive layers; and

a plurality of the semiconductor components mounted to the interconnect with a plurality of second contacts on the components electrically engaging the plurality of first contacts on the interconnects.

76. The module of claim 75 wherein the first contacts comprise raised members with penetrating members and the second contacts comprise planar bond pads.

77. The module of claim 75 wherein the first contacts comprise recesses at least partially covered by the conductive layers and configured to retain the first contacts.